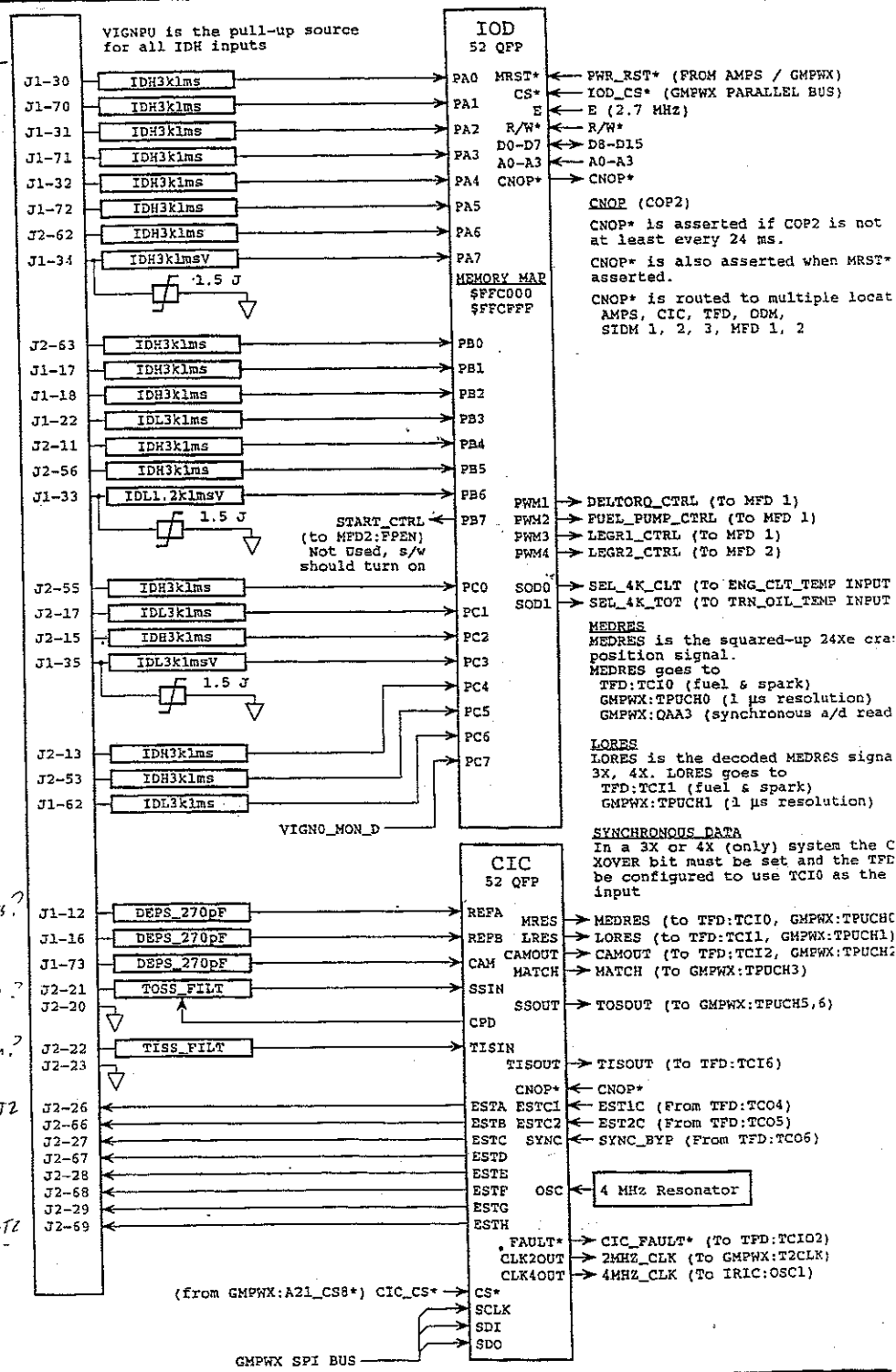


DI to port bias

Hall effects?
" "
" "
OR Fin?
or Fin?

5V pushpull 4mA ESTZ
spark out
ESTZ



SIDMS

The SIDM chip selects are sourced by the GMPWX:PCS ports. SIDMS can be updated at high speed via the QSPI architecture with minimal CPU overhead.

Software should command SIDM2_OUT4 and SIDM1_OUT2,3,4 on in order to prevent false open-circuit fault indications.

Outputs used as discretes should be set at maximum frequency in order to minimize update delay times.

32KHZ_CLK is sourced by TFD:TCO1 and is the time base for SIDM PWM outputs (32.90 kHz).

Assertion of CNOP* disables all outputs. Loss of 32KHZ_CLK also disables all outputs.

ODM

The ODM chip select is sourced by the GMPWX:FCO_CS3* output which is configured as a discrete output.

Assertion of CNOP* disables all outputs except OUT1.

Periodic polling of the ODM SPI data should be used to assess ODM fault status.

MALF_IND_CTRL

The source for this signal is GMPWX:IRQ7*.

After reset IRQ7* is the highest priority interrupt (input). Software must re-configure IRQ7* as a discrete output after reset.

The pull-up resistor is required to prevent IRQ7* from interrupting the processor at power-up, and also assures that if the processor is in reset the MIL light will be on (CNOP* doesn't affect OUT1).

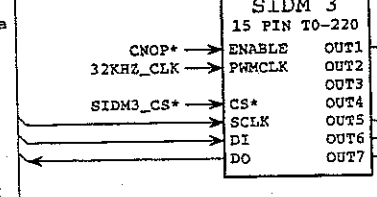
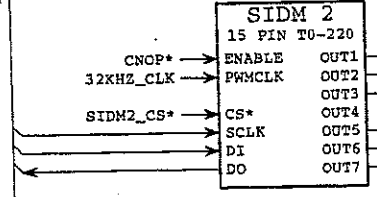
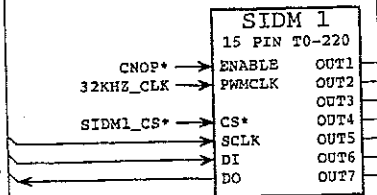
ODM FLT*

(to TFD:TCIO3)

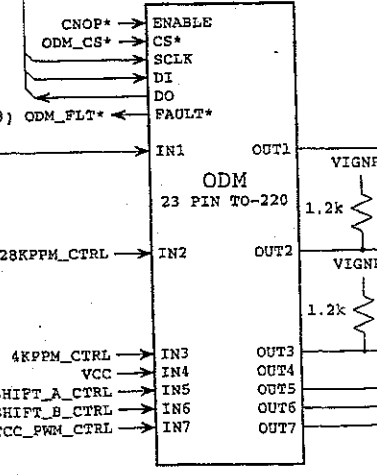
After reset AVEC* is configured as an input and RMC* is configured as an output (and is high).

Software should properly configure these signals prior to releasing CNOP* (COP toggling) in order to prevent a glitch on the SHIFT_B output.

GMPWX SPI BUS



CRUISE INH*
This is a low-side-drive output and thus active low. However, system level definition requires an open wire to inhibit cruise. Therefore, to allow cruise, the output must be turned on (low).



Connector Notes
J1 = J1-F (schematic)
J2 = J1-S (schematic)
J1 (J1-F_) = BLUE
J2 (J1-S_) = RED

J2-36 0LS32 DO
J2-37 0LS32 DO
J2-35 0LS32 (400mA) PWM
J2-38 0LS32 (700mA) PWM
J2-34 0LS20
J2-33 0LS20
J1-42 0LS10 (1.9A)

J1-38 0LS32 DO
J1-39 0LS32 DO
J2-4 0LS32
J2-3 0LS20
J1-78 0LS20
J1-79 0LS10 (1.9A) FAN

J2-43 0LS32 (DO)

J2-44 0LS20
J2-45 0LS20
J2-42 0LS10 (1.9A) FAN

J2-46 0LS32 (DO) (can be on during Reset)

J2-49 0LS32 900mA (Freq)

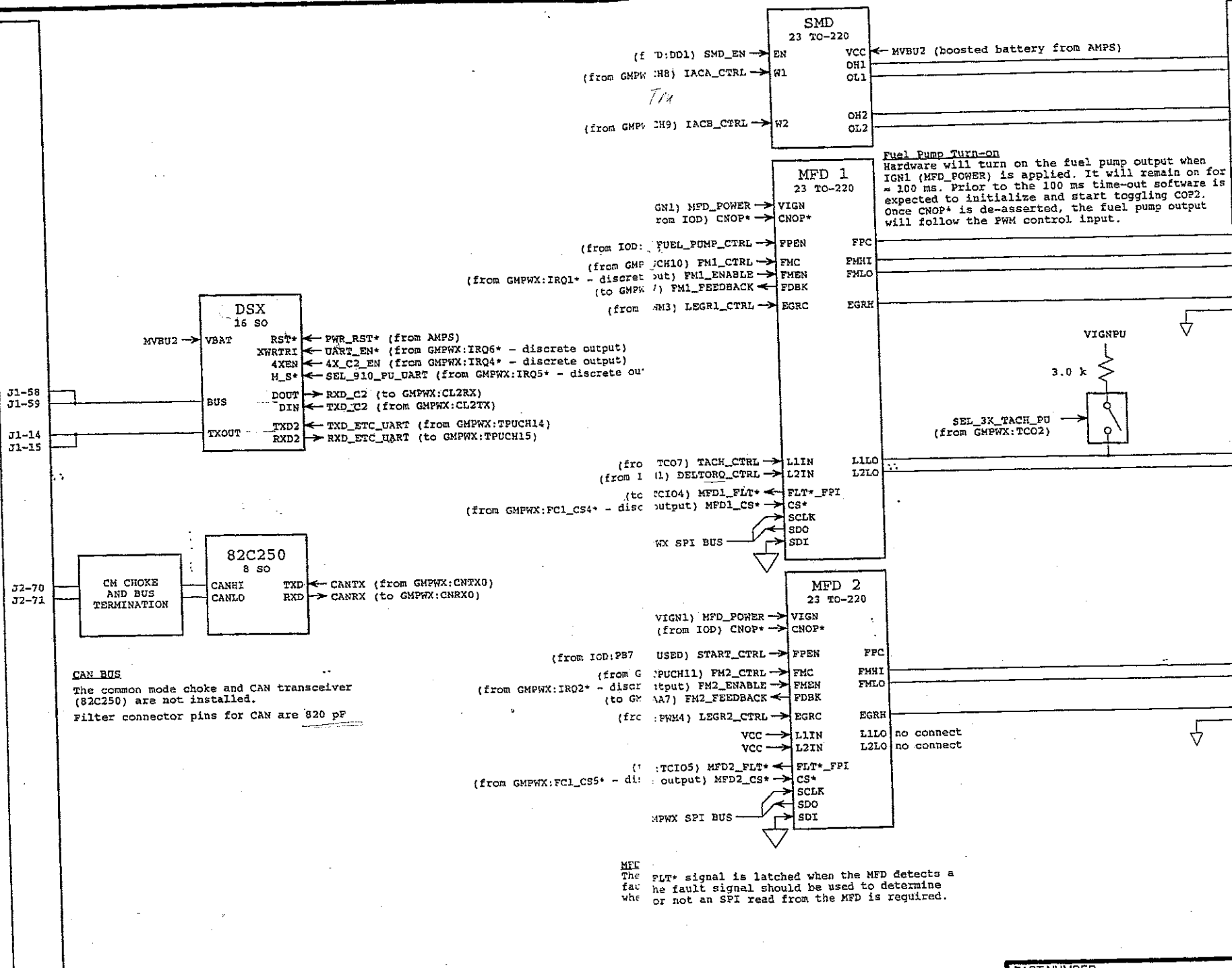
J2-50 0LS32 900mA (Freq)

J2-48 0LS20 (DO)
J2-47 0LS20 (DO)
J2-2 0LS10 1.9A (pwm)

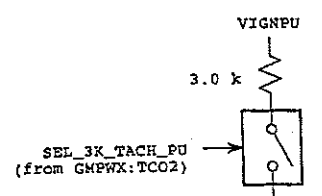
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CAN



Fuel Pump Turn-on
 Hardware will turn on the fuel pump output when IGN1 (MFD POWER) is applied. It will remain on for ~ 100 ms. Prior to the 100 ms time-out software is expected to initialize and start toggling COP2. Once CNOP* is de-asserted, the fuel pump output will follow the PWM control input.



Connector Notes
 J1 = J1-F_ (schematic)
 J2 = J1-S_ (schematic)
 J1 (J1-F_) = BLUE
 J2 (J1-S_) = RED

OH528 (Relay driver)
 FMTR HI 1.1A
 FMTR LO 1.1A
 1.1A LECR H50

J2-10 OL5500 (30mA)
 J2-5 OL5500 (30mA)

J2-75 FMTR HI
 J2-72 FMTR LO
 1.1A LECR H50

MEF
 The FLT* signal is latched when the MFD detects a fault. The fault signal should be used to determine when or not an SPI read from the MFD is required.

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